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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/407,204	09/28/99	SHEN M	8688.128US01

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MMC2/1222

EXAMINER
PAREKH, N

ART UNIT	PAPER NUMBER
2811	7

DATE MAILED: 12/22/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/407,204	Shen
Examiner	**Group Art Unit**
Nitin Parekh	2811

☒ Responsive to communication(s) filed on *Nov 22, 1900*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-6 and 19* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-6 and 19* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☒ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Londa (US Pat. 6101100) in view of Clayton (US Pat. 5731633) and Panchou et al (US Pat. 6040630) and in further view of Bertin et al (US Pat. 5977640).

Regarding claims 1 and 2, Londa discloses a semiconductor chip module/stack comprising:

- an upper and lower semiconductor chip modules

- a chip mounting member/composite substrate (12, 30 and 22 in Fig. 2) having opposite first and second surfaces (14 and 26 in Fig. 2), a set of circuit traces (20 and 27 in Fig. 2) , a plurality of plated through holes that extend through the first and second surfaces and are connected to the circuit traces (42, 44, etc. in Fig. 2)

- a first and second semiconductor chips (36 and 40 respectively in Fig. 2) having a pad mounting surface with a plurality of contact pads (38a, 38b, etc. in Fig. 2) provided thereon and the chip secured/fixed to the chip mounting member

- a first and second conductor units (102a, 102c respectively in Fig. 2) for electrically connecting the contact pads of the first semiconductor chip and first circuit traces, and

- plurality of solder balls disposed on one of the surfaces of the chip mounting member, each one being aligned and connected to the respective one of the plated through holes in the chip mounting member (66, 68, etc. in Fig. 2) and aligned and connected to those of the upper and lower semiconductor chip modules

(Fig. 1 and 2; Col. 3, line 35- Col. 5, line 3).

Londa discloses the first semiconductor chip being secured/fixed to the chip mounting member/substrate (Col. 3, line 58) but fails to specify using a first dielectric tape for bonding/securing adhesively with the a plurality of holes at positions registered with the first conductor unit including a plurality contact pads/balls of the first semiconductor chip to bond and establish the electrical connection between the chip to the first circuit traces on the chip mounting member/substrate. Clayton teaches using the conventional adhesive film/dielectric tape for bonding the first and second semiconductor chips on the circuit substrate (Fig. 18A-D; Col.. 11, line 36; Col. 18, line 50) in a multichip module with wire bonding (Fig. 18C) or flip chip bonding (Fig. 18D). Clayton further teaches disposing the first circuit traces and the first semiconductor chip on the same surface of the chip mounting member/substrate and the forming the bonding with the contact pads/balls being registered with those of the chip and the substrate (74 and 76 in Fig. 18D; Col. 19, line 33) in flip chip bonding. Panchou et al teach using a conventional attachment film/dielectric tape with a plurality of holes at positions in registration with the

corresponding contact pads/balls of the chip in adhesive bonding of a flip chip device (Fig. 4 and 4a; Col. 5; Fig. 1-4). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to use a first dielectric tape for bonding/securing adhesively with a plurality of holes at positions registered with the first conductor unit including a plurality contact pads/balls of the first semiconductor chip to bond and establish the electrical connection between the chip to the first circuit traces on the chip mounting member/substrate to improve the chip bonding using Clayton and Panchou et al's teachings in Londa as cited in claims 1 and 2.

Regarding claims 3 and 4, Londa fails to specify using a second dielectric tape with a plurality of holes at positions registered with the plurality of balls of the second semiconductor chip to bond and establish the electrical connection between the second semiconductor chip to the second circuit traces on chip mounting member/substrate. However, as explained above for claims 1 and 2, Londa in view of Clayton and Panchou et al further teaches using the second semiconductor chip, second dielectric tape with a plurality of holes and the second conductor unit including plurality of conductive pads/balls in registration with the corresponding holes in the tape. Therefore, claims 3 and 4 are rejected as explained above for claims 1 and 2.

Regarding claim 5, Londa discloses providing an epoxy resin (104 in Fig. 2; Col. 4, line 58) to strengthen the bonding of the first semiconductor chip with the same one of the surfaces of the chip mounting member/substrate.

Regarding claim 6, Londa in view of Clayton and Panchou et al fails to specify securing a heat dissipating plate on the heat dissipating surface opposite to the pad mounting surface of the chip. Bertin et al teach using conventional heat spreader/plate secured on the heat dissipating surface opposite to the pad mounting surface of the chip (Fig. 7 and 15; Col. 4, line 16) to improve heat dissipation. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a heat dissipating plate on the heat dissipating surface opposite to the pad mounting surface of the chip to improve heat dissipation using Bertin et al's heat spreader in Londa's module in view of Clayton and Panchou et al as cited in claim 6.

The combined teachings of Londa, Clayton, Panchou et al and Bertin et al apply to claim 19 as explained above for claims 1-4.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

12-17-00

Tom Thomas